

## **REMARKS**

Claims 1, 3-4, 6-12, and 14-30 are pending in the application. Claims 1, 3-4, 6-12, and 14-15 are allowed. Claims 16-18, 21-23, and 26-29 are rejected. Claims 19-20, 24-25, and 29-30 are objected to as being dependent on a rejected base claim, but would be allowable if rewritten in independent form. Claims 1, 3-4, 6-12, and 14-15 have been amended to correct grammatical and typographical errors and to improve clarity. Claims 16-21, 24-26, and 29-30 have also been amended.

Claims 16-17 were rejected under 35 U.S.C. §103(a) as being unpatentable over Horstmann et al, U.S. Patent No. 6,125,433 (hereinafter “Horstmann”) in view of Watkins et al, U.S. Patent No. 5,937,436 (hereinafter “Watkins”). Claim 18 was rejected under 35 U.S.C. §103(a) as being unpatentable over Horstmann in view of Watkins in further view of Futral et al, U.S. Patent No. 6,112,263 (hereinafter “Futral”). Claims 21-23 and 26-28 were rejected under 35 U.S.C. §103(a) as being unpatentable over Watkins in view of Horstmann in further view of Futral.

### **Claim Rejections Under 35 U.S.C. §103(a)**

Claims 16-17 were rejected under 35 U.S.C. §103(a) as being unpatentable over Horstmann in view of Watkins. Horstmann discloses an optimized translation lookaside buffer (TLB) utilizes a least-recently-used algorithm for determining the replacement of virtual-to-physical memory translation entries (See Abstract). Watkins discloses a network interface circuit including an address translation unit and a flush check circuit, and a method for checking for an invalid address translation within of the address translation unit (See Abstract).

Applicants contend that Horstmann, Watkins, and any combination thereof fail to teach or suggest each of said TPT entries including protection attributes to control read and write access to a given memory region of a host memory and a memory protection tag to specify whether said apparatus has permission to access said host memory, as recited in claim 16 as amended.

Therefore, claim 16 and by its dependency claim 17, are not obvious under Horstmann in view of Watkins.

Claim 18 was rejected under 35 U.S.C. §103(a) as being unpatentable over Horstmann in view of Watkins in further view of Futral. Futral discloses an I/O device driver shared between a number of processes within a computer system while security and protection for system memory is maintained (See Abstract).

Applicants contend Horstmann, Watkins, Futral, and any combination thereof fail to teach or suggest each of said TPT entries including protection attributes to control read and write access to a given memory region of a host memory and a memory protection tag to specify whether said apparatus has permission to access said host memory, as recited in claim 16 as amended.

Therefore, claim 18 by its dependency on claim 16, is not obvious under Horstmann in view of Watkins in further view of Futral.

Claims 21-23 and 26-28 were rejected under 35 U.S.C. §103(a) as being unpatentable over Watkins in view of Horstmann in further view of Futral.

Applicants contend that Horstmann, Watkins, Futral, and any combination thereof fail to teach or suggest each of the TPT entries comprising a memory protection tag to specify whether the adapter has permission to access the host memory.

Therefore, claims 21 and 26 and by their dependency claims 22-23 and 27-28, are not obvious under Watkins in view of Horstmann in further view of Futral.

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. **11-0600**.

Respectfully submitted,

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